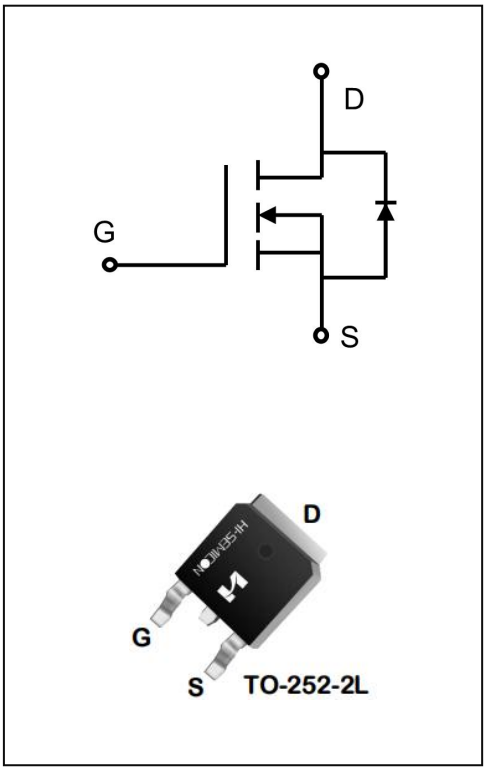
8A, 650V N-CHANNEL MOSFET



GENERAL DESCRIPTION

These N-Channel enhancement mode power field effect transistors are produced using Hi-semicon's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

- ◆VDS(V)=650V, ID=8A
- ◆$R_{DS(ON)}$
  TYP:1.15Ω@V_{GS}=10V I_D=4.0A
  MAX:1.4Ω

Applications

- ◆used in various power switching circuit for system miniaturization and higher efficiency
- ◆Power switch circuit of electron ballast and adaptor

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFD8N65	TO-252-2L	SFD8N65	Pb Free	Reel

ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise noted)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C = 25°C	I_D	8.0	A
	T_C = 100°C		5.6	
Drain Current Pulsed (Note 1)		I_{DM}	32	A
Power Dissipation(T_C=25°C)		P_D	105	W
-Derate above 25°C			0.84	W/°C
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	605	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C
Maximum lead temperature for soldering purposes,1/8" from case for 5 seconds		TL	300	℃

THERMAL CHARACTERISTICS

Characteristics	Symbol	MAX	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.19	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	3.0	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=4.0A	--	1.15	1.4	Ω
Forward Trans conductance	gfs	V_{DS}=10V, I_D=5.0A	--	9.5	--	S
Dynamic Characteristics						
Gate Resistance	Rg	V_{GS}=0V; f=1.0MHZ	--	3.5	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V V_{GS}=0V f=1.0MHZ	--	1100	--	pF
Output Capacitance	C_{oss}		--	47	--	
Reverse Transfer Capacitance	C_{rss}		--	6.0	--	pF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=400V; V_{GS}=10V R_G=12Ω; I_D=4A (Note 3.4)	--	13.1	--	ns
Turn-on Rise Time	t_r		--	14.8	--	
Turn-off Delay Time	$t_{d(off)}$		--	47.6	--	
Turn-off Fall Time	t_f		--	49.2	--	

Total Gate Charge	Q_g	V_{DS}=650V, I_D=4A	--	25.7	--	nc
Gate-Source Charge	Q_{gs}	V_{GS}=10V	--	5.4	--	
Gate-Drain Charge	Q_{gd}	(Note 3.4)	--	9.6	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	8	A
Pulsed Source Current	I_{SM}		--	--	32	
Diode Forward Voltage	V_{SD}	I_S=8A,V_{GS}=0V	--	--	1.2	V
Reverse Recovery Time	T_{rr}	I_F=4A,V_R=400V, dIF/dt=100A/μS	--	352	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.47	--	μC

1.Pluse width limited by maximum junction temperature

2.L=10mH, I_{AS}=12A, V_{DD}=100V, V_G=10V, R_G=25Ω, starting T_J=25°C

3.Pulse Test: Pulse width ≤300μs, Duty cycle≤2%

4.Essentially independent of operating temperature

Typical Performance Characteristics

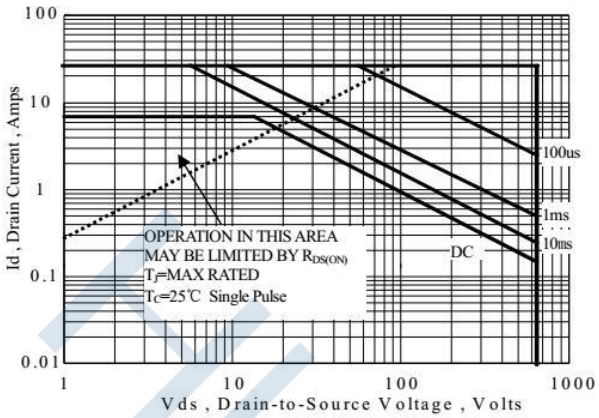


Figure 1 Maximum Forward Bias Safe Operating Area

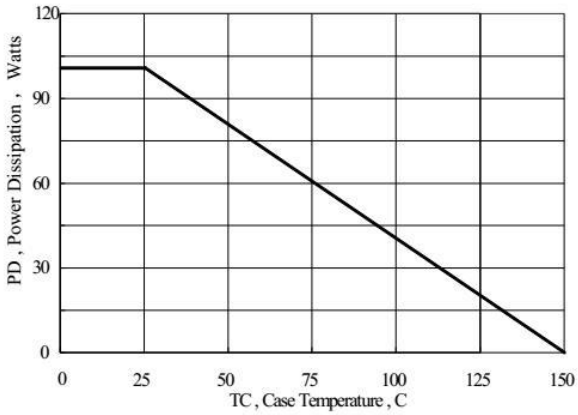


Figure 2 Maximum Power Dissipation vs Case Temperature

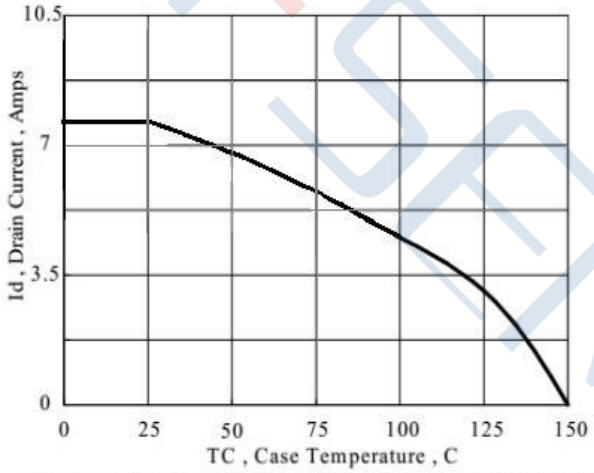


Figure 3 Maximum Continuous Drain Current vs Case Temperature

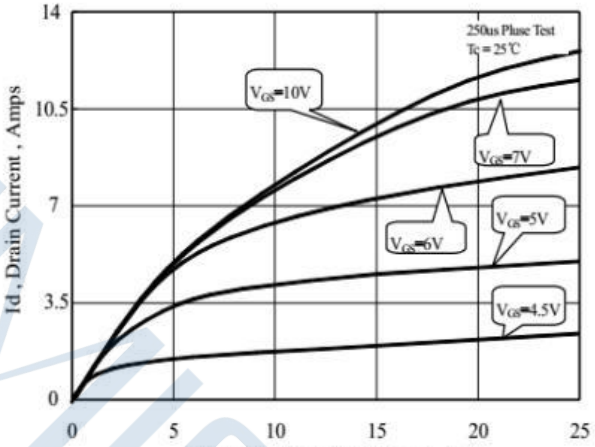


Figure 4 Typical Output Characteristics

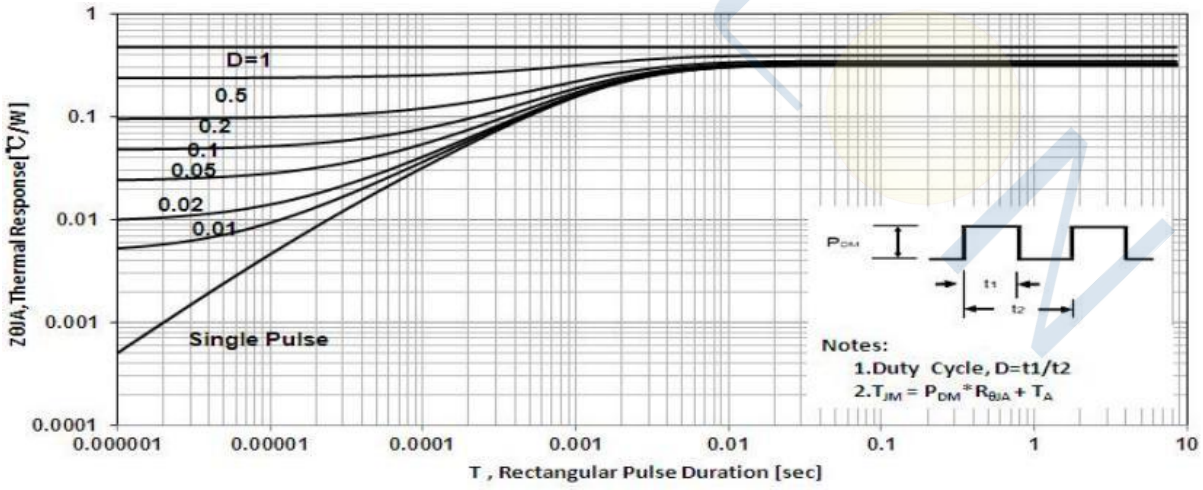


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

Typical Performance Characteristics

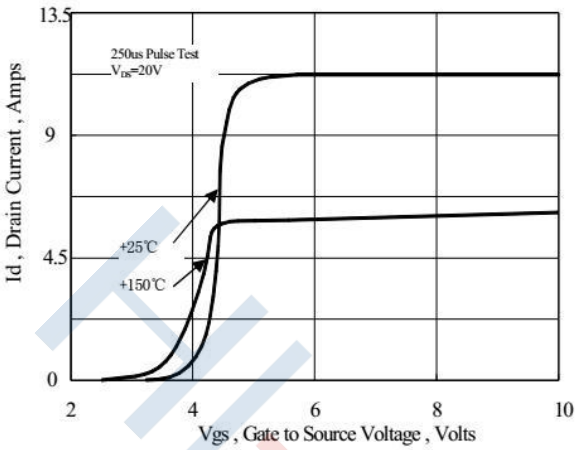


Figure 6 Typical Transfer Characteristics

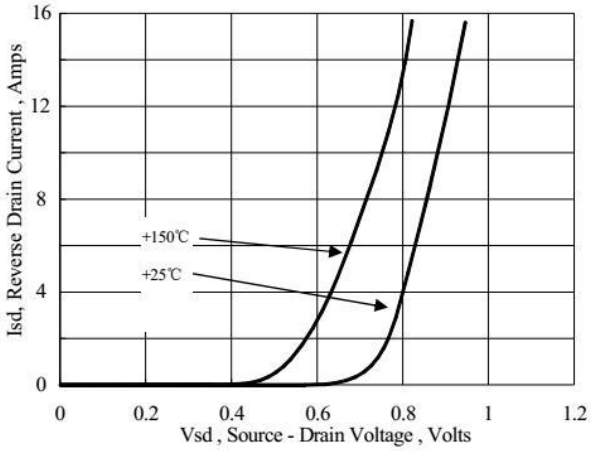


Figure 7 Typical Body Diode Transfer Characteristics

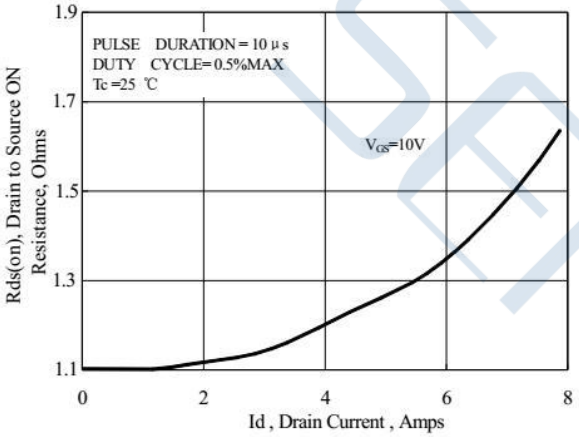


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

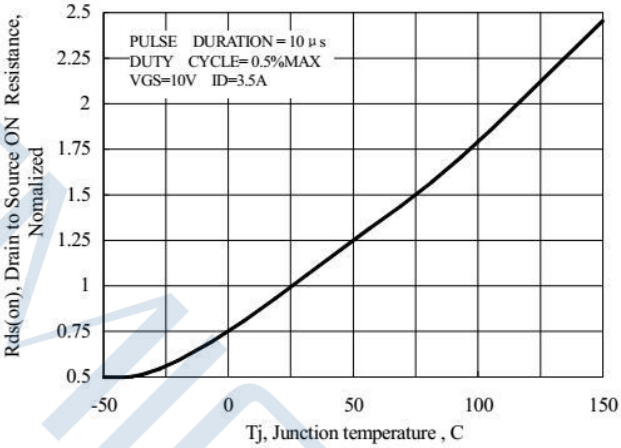


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

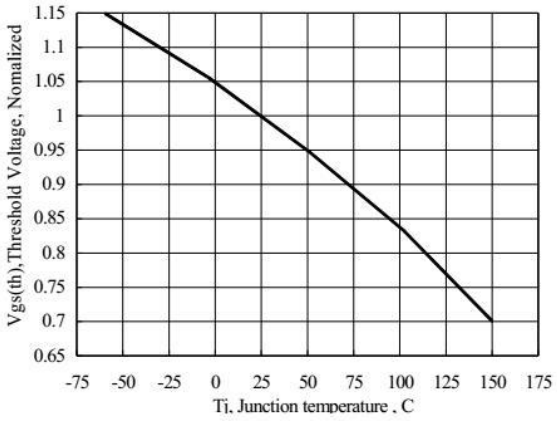


Figure 10 Typical Theshold Voltage vs Junction Temperature

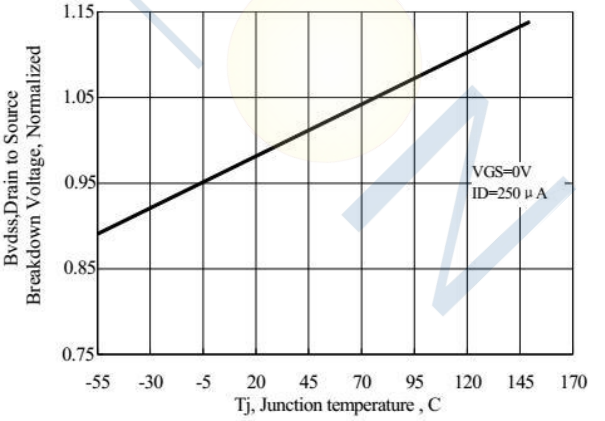


Figure 11 Typical Breakdown Voltage vs Junction Temperature

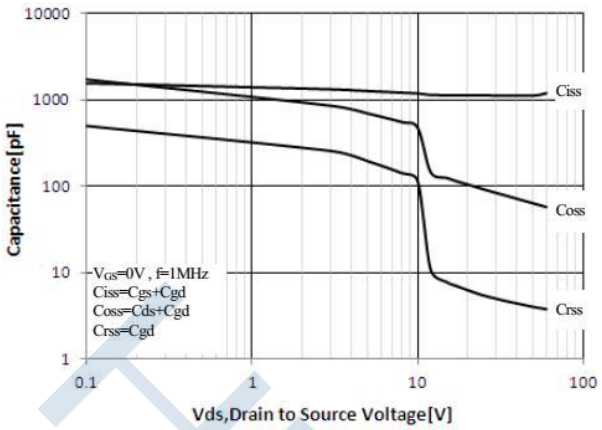


Figure 12 Typical Capacitance vs Drain to Source Voltage

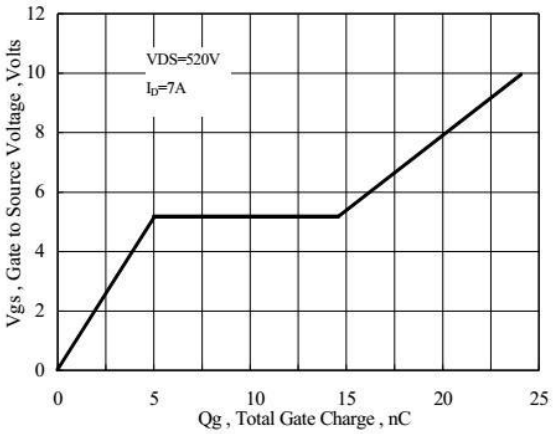


Figure 13 Typical Gate Charge vs Gate to Source Voltage

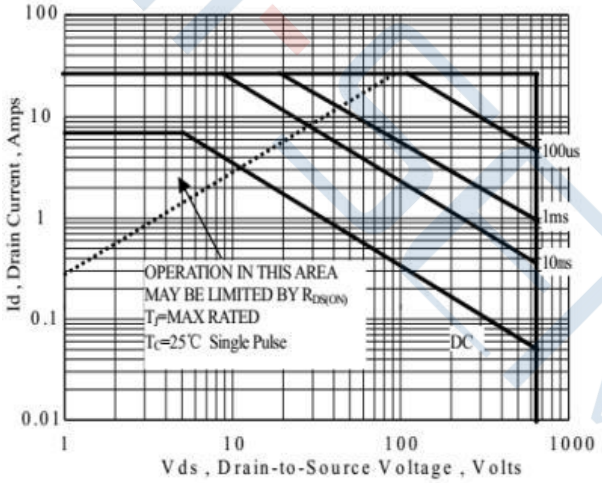


Figure 14 Maximum Forward Bias Safe Operating Area

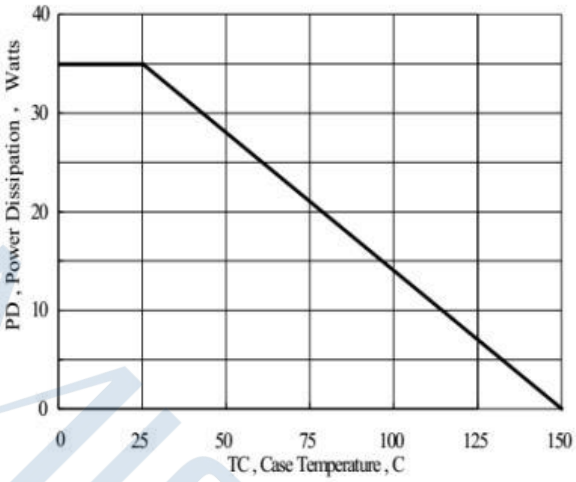
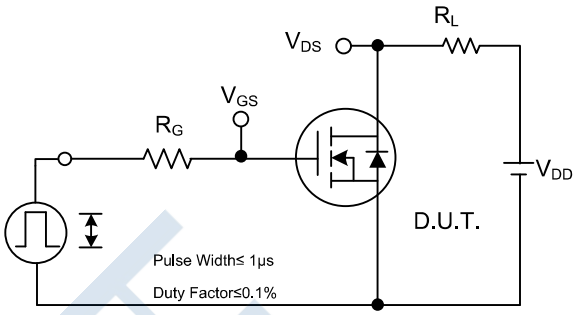
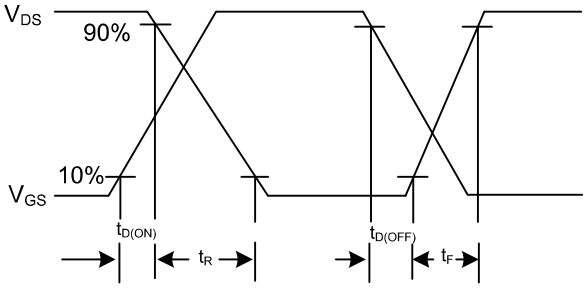


Figure 15 Maximum Power Dissipation vs Case Temperature

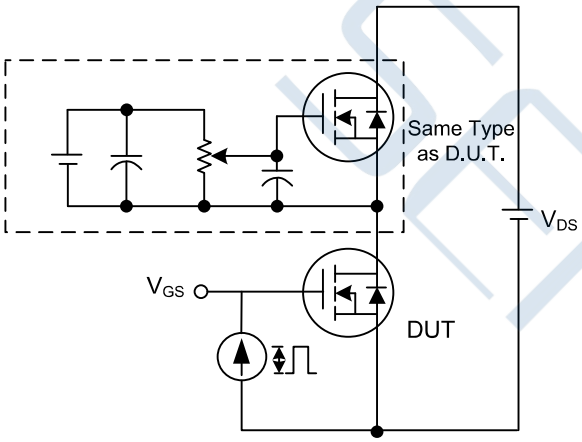
Test Circuit



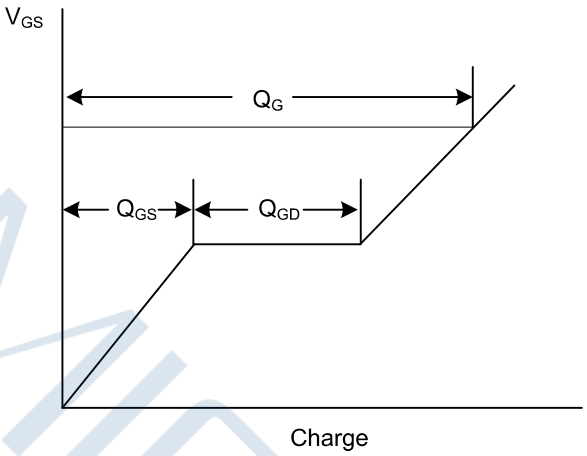
Switching Test Circuit



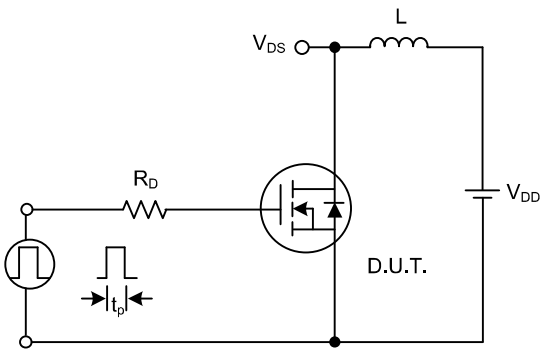
Switching Waveforms



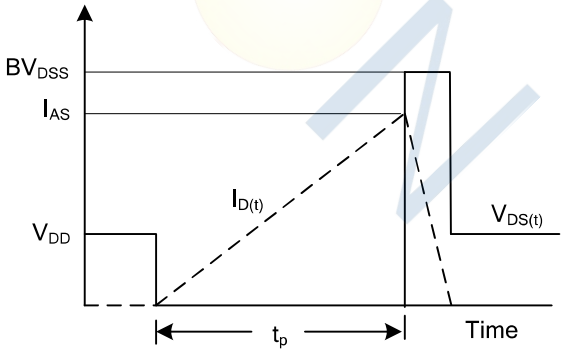
Gate Charge Test Circuit



Gate Charge Waveform



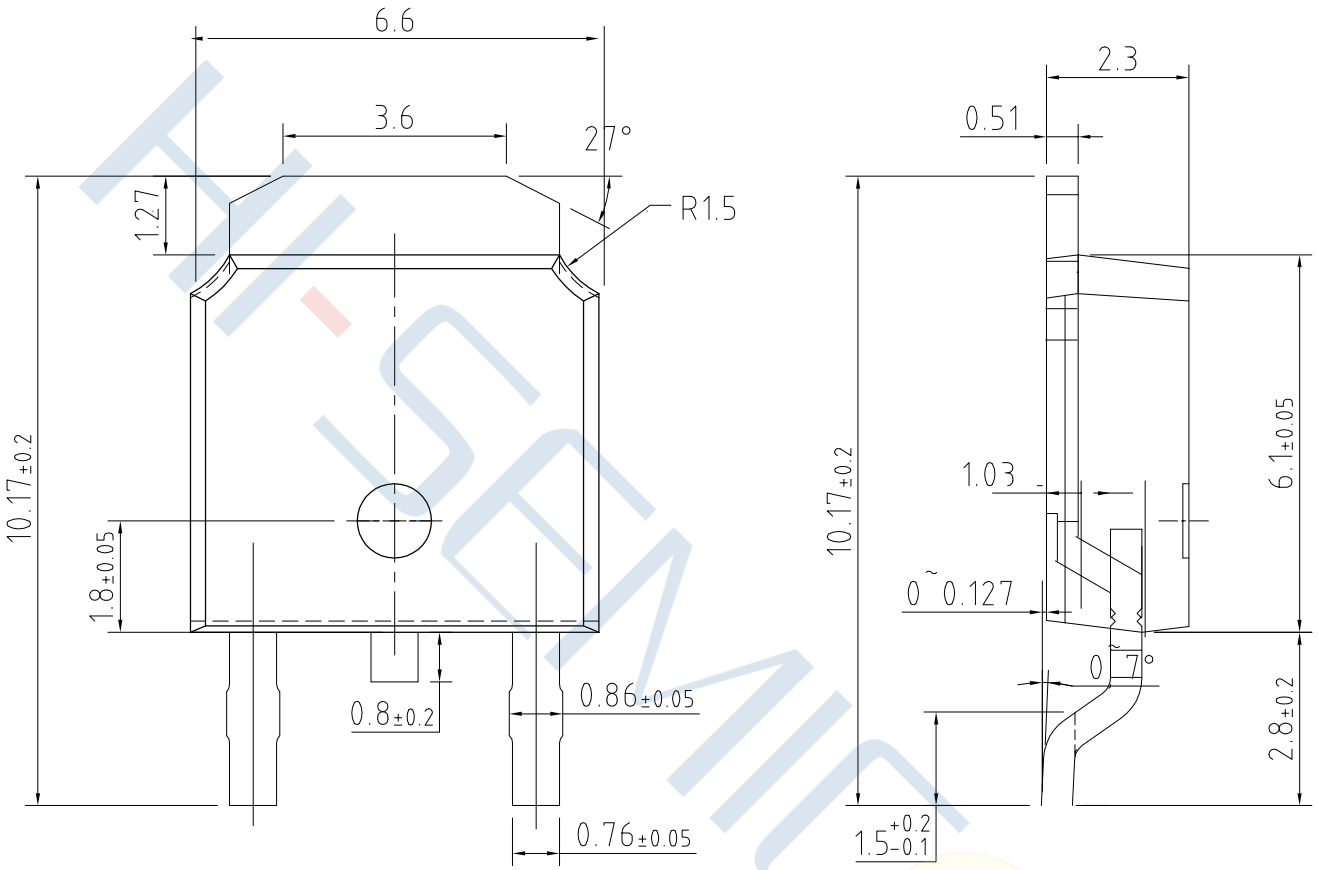
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Package Dimensions of TO-252-2L

Unit:mm



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