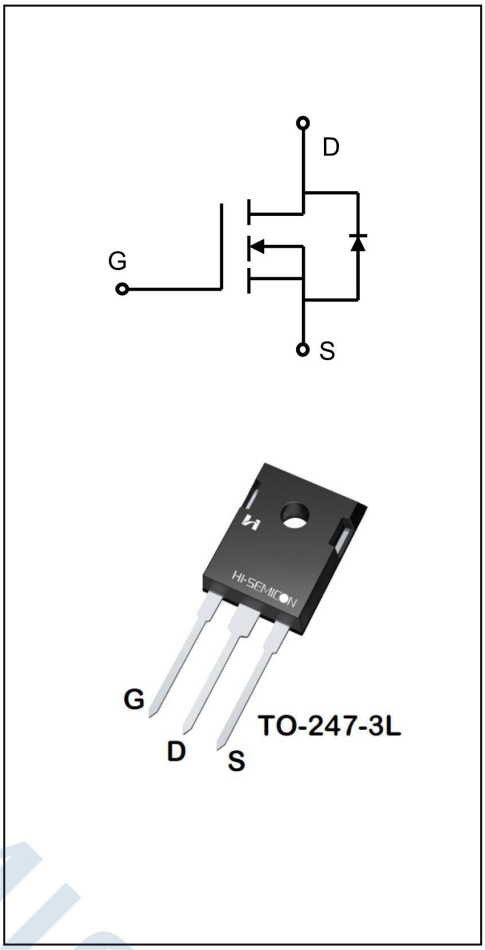
50A, 250V N-CHANNEL MOSFET



GENERAL DESCRIPTION

This power mosfet is an N-channel enhancement mode power MOS field effect transistor which is produced using Hi-semicon proprietary F-CellTM structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

Features

◆V_{DS}(V)=250V, I_D=50A

◆$R_{DS(ON)}$

TYP:48mΩ@V_{GS}=10V

MAX:60mΩ

Applications

◆Power faction correction (PFC)

◆Uninterruptible power supply (UPS)

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFW50N25	TO-247-3L	SFW50N25	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise noted)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	250	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C = 25°C	I_D	50	A
	T_C = 100°C		35	
Drain Current Pulsed (Note 1)		I_{DM}	200	A
Power Dissipation(T_C=25°C)		P_D	223	W
-Derate above 25°C			1.78	W/°C
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	841	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C
Maximum lead temperature for soldering purposes,1/8" from case for 5 seconds		TL	300	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	MAX	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.56	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	250	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=250V, V_{GS}=0V	--	--	1.0	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=-30V, V_{DS}=0V	-100	--	--	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	3.3	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=25A	--	48	60	mΩ
Forward Transconductance	gfs	VDS = 20V, ID = 25A	--	15	--	S
Dynamic Characteristics						
Gate Resistance	Rg	V_{GS}=0V; f=1.0MHZ	--	2.8	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V	--	5183	--	pF
Output Capacitance	C_{oss}	V_{GS}=0V	--	538	--	
Reverse Transfer Capacitance	C_{rss}	f=1.0MHZ	--	18	--	
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	VDD = 125V, ID = 50A, VGS =10V.RG = 10Ω (Note 3.4)	--	43.4	--	ns
Turn-on Rise Time	t_r		--	123.3	--	
Turn-off Delay Time	$t_{d(off)}$		--	48.8	--	
Turn-off Fall Time	t_f		--	93.9	--	

Total Gate Charge	Q_g	VDD = 200V,	--	83.7	--	nc
Gate-Source Charge	Q_{gs}	ID = 50A,V_{GS}=10V	--	32.7	--	
Gate-Drain Charge	Q_{gd}	(Note 3.4)	--	23.2	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	50	A
Pulsed Source Current	I_{SM}		--	--	200	
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_F=50A,V_{GS}=0V, dIF/dt=100A/μS	--	180	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.42	--	μC

1.Pluse width limited by maximum junction temperature

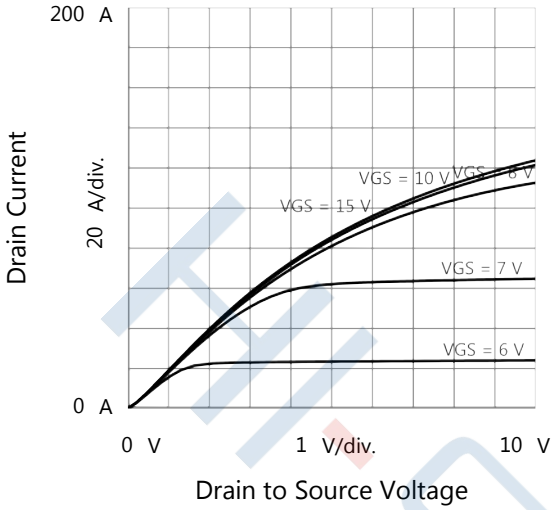
2.L=0.5mH, I_{AS}=58A, V_{DD}=50V, V_G=10V, R_G=25Ω, starting T_J=25°C

3.Pulse Test: Pulse width ≤300μs, Duty cycle≤2%

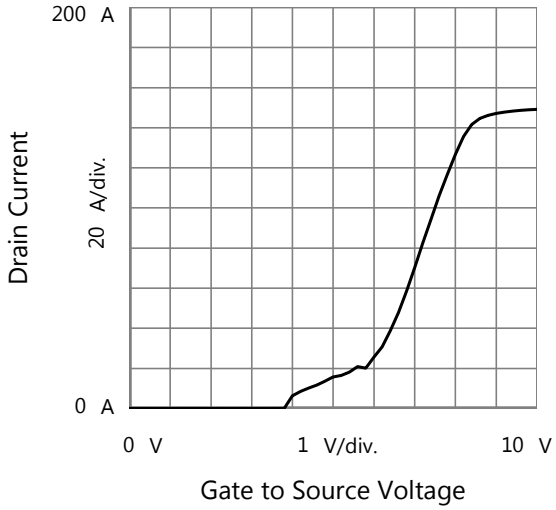
4.Essentially independent of operating temperature

Typical Performance Characteristics

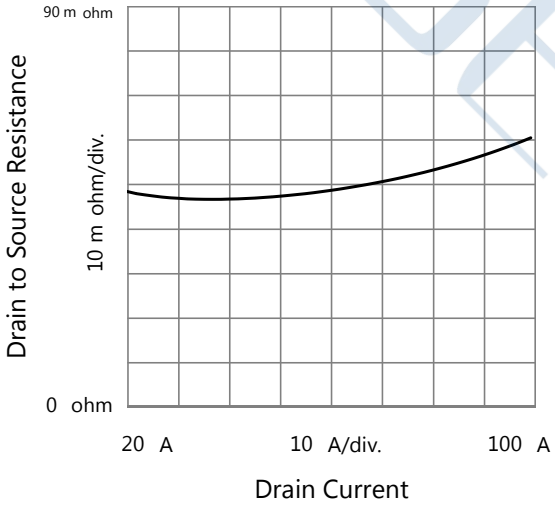
Output Characteristics



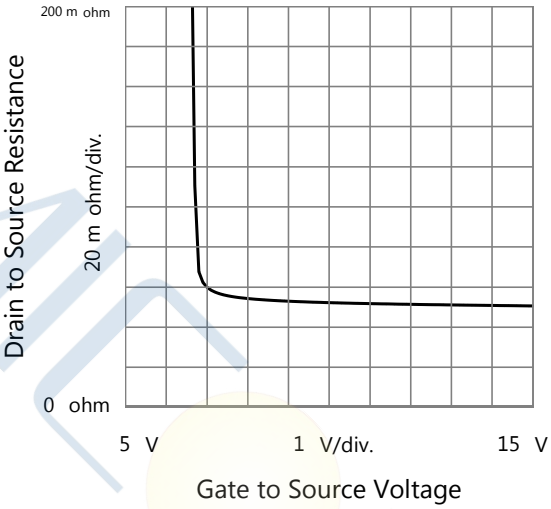
Transfer Characteristics



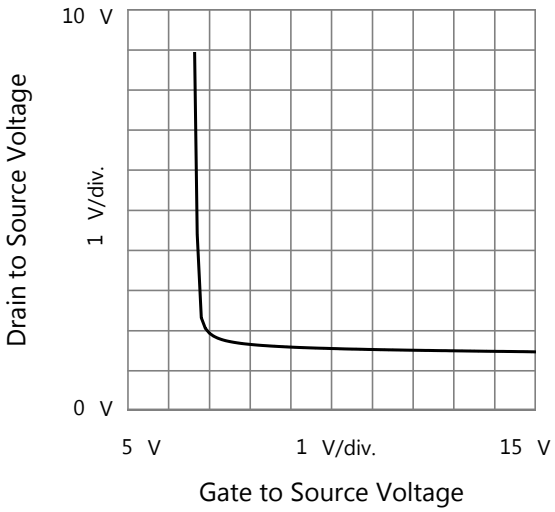
Drain to Source Resistance vs. Drain Current



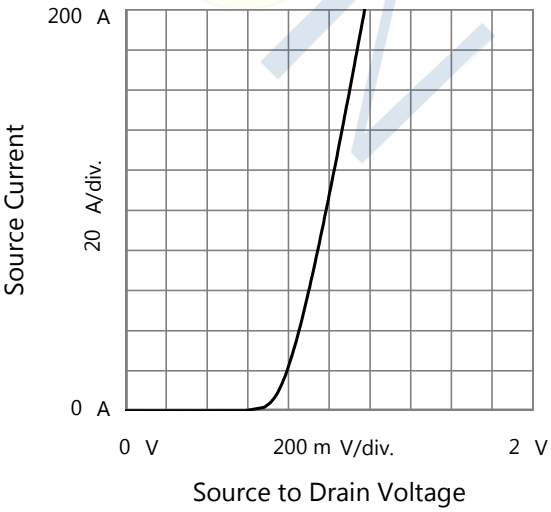
Drain to Source Resistance vs. Gate to Source Voltage



Drain to Source Voltage vs. Gate to Source Voltage

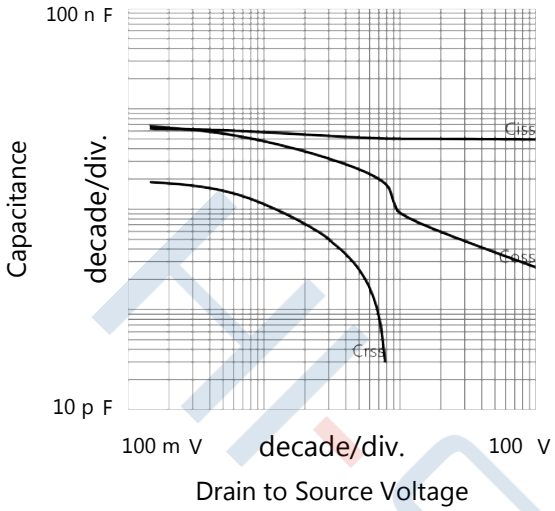


Body Diode Forward Characteristics

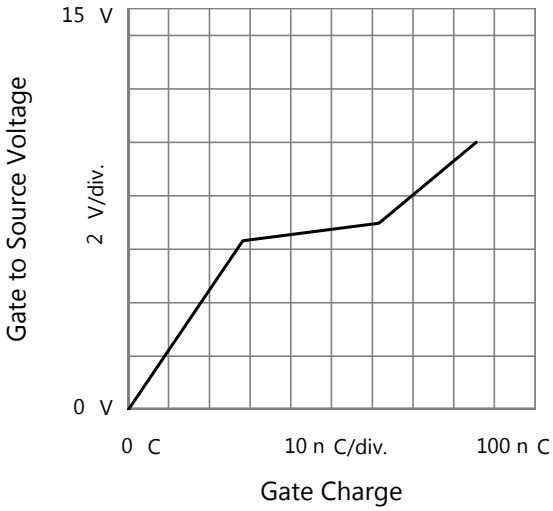


Typical Performance Characteristics

Capacitances



Gate Charge



Test Circuit

Figure A: Gate Charge Test Circuit and Waveform

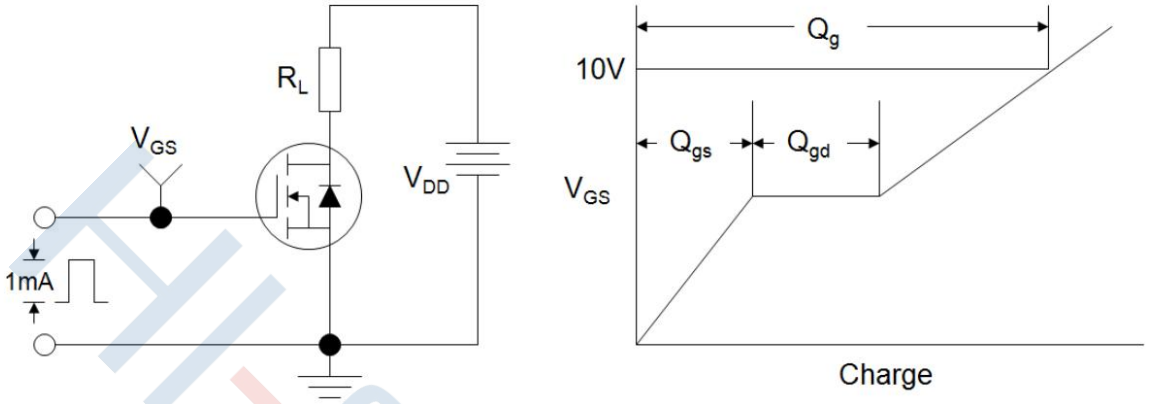


Figure B: Resistive Switching Test Circuit and Waveform

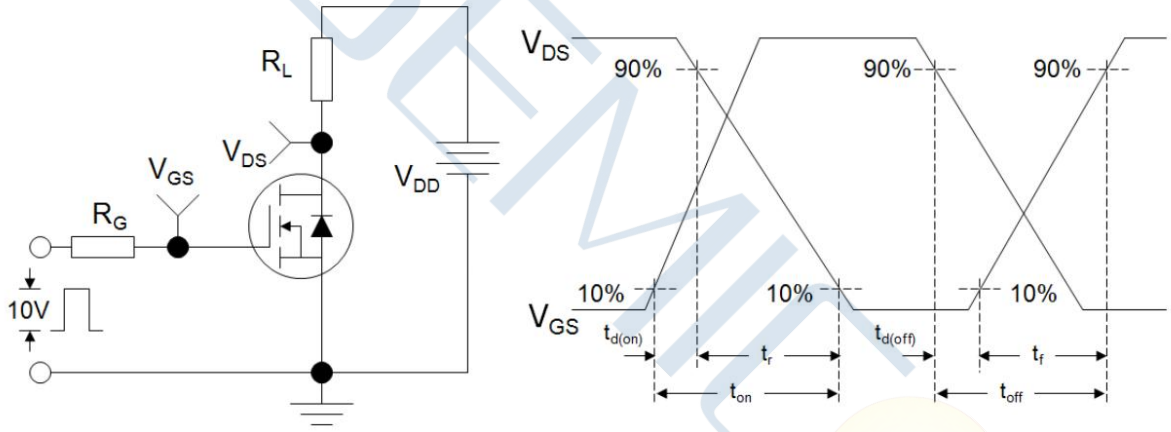
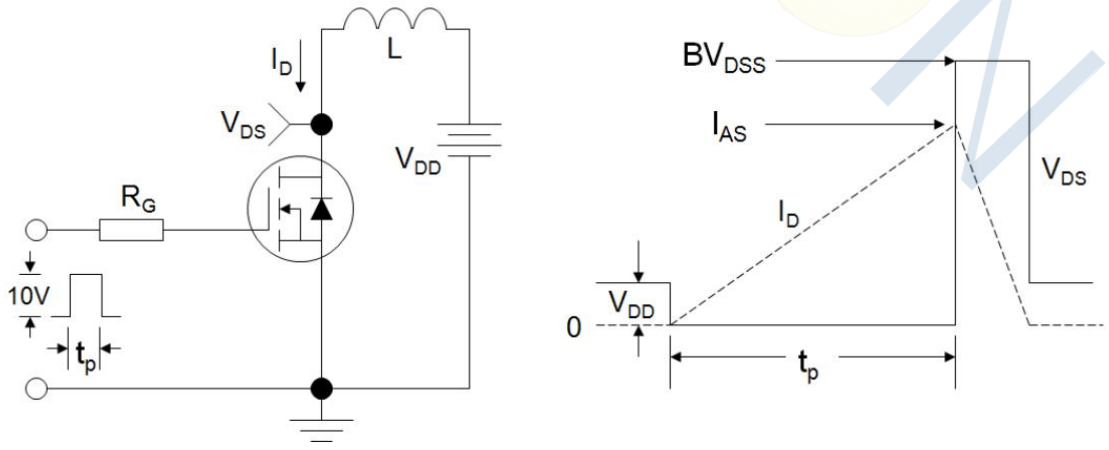
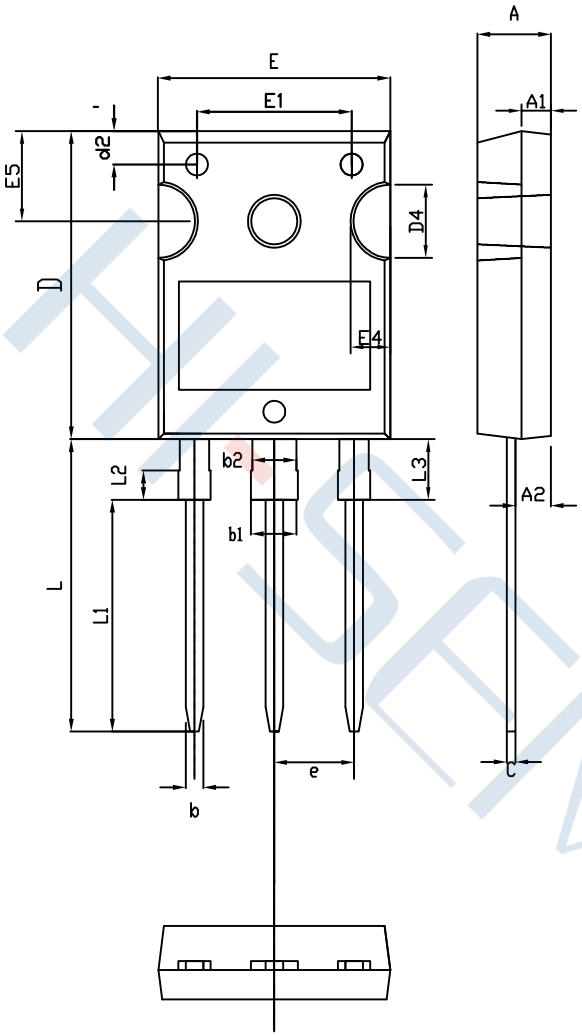


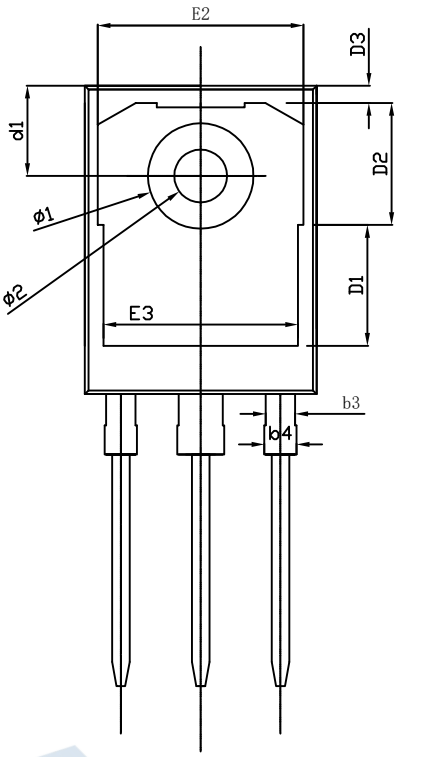
Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package Dimensions of TO-247-3L

Unit:mm





	MIN	NOM	MAX
A	4.60	4.80	5.00
A1	1.90	2.00	2.10
A2	2.27	2.41	2.54
b	1.10	1.20	1.30
b1	2.90	-	3.20
b2	2.90	3.00	3.10
b3	1.90	2.00	2.10
b4	2.00	-	2.20
c	0.55	0.60	0.68
D	20.80	21.00	21.10
D1		8.23	
D2		8.32	
D3		1.17	
D4	3.68	4.90	5.10
d1	6.04	6.15	6.30
d2	2.20	2.30	2.40
E	15.70	15.80	16.00
E1		10.50	
E2		14.02	
E3		13.50	
E4	2.20	2.40	2.60
E5	5.49	5.80	6.00
e	5.34	5.44	5.54
L	19.72	19.92	20.12
L1		15.79	
L2		1.98	
L3	4.00	4.10	4.47
⌀1	7.10	7.19	7.30
⌀2	3.50	3.60	3.70

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